

# Overlapped List Successive Cancellation Approach for Hardware Efficient Polar Code Decoder

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**Abstract**—This paper presents an efficient hardware design approach for list successive cancellation (LSC) decoding of polar codes. By applying path-overlapping scheme, the  $l$  instances of ( $l > 1$ ) successive cancellation (SC) decoder for LSC with list size  $l$  can be cut down to only one. This results in a dramatic reduction of the hardware complexity without any decoding performance loss. We also develop novel approaches to reduce the latency associated with the pipeline scheme. Simulation results show that with proposed design approach the hardware efficiency is increased significantly over the recently proposed LSC decoders.

## I. INTRODUCTION

Recently, polar codes [1] have received significant attention due to its capability to achieve the capacity of binary-input memoryless symmetric channels with low-complexity encoding and decoding schemes. E. Arikan in [1] presents a recursive cancellation way to successively accomplish decoding; and this method is referred to successive cancellation (SC). Also, N. Hussami et al. in [2] shows that the belief propagation (BP) can be applied as decoding algorithm. However, the decoding performances of both SC and BP are inferior to that of low density parity check (LDPC) codes. In order to make polar codes more competitive, the list SC (LSC) decoding algorithm is presented in [3]. By exploiting a larger range in the codeword tree, LSC significantly improves the decoding performance.

Attracted by the potentials of LSC, a number of relevant hardware designs have been explored. In [4], hardware LSC architectures of list sizes two and four are proposed with pointer memory technique, which can avoid the high complexity of likelihood copying. In [5], a hardware efficient architecture of LSC concatenated with cyclic redundancy check (CRC) is presented. In [6], a hardware architecture of sub-optimal version of LSC decoding is introduced. In [7], a LSC with multi-bit decision is discussed, which significantly reduces the decoding latency, and the corresponding hardware architecture is presented. All of aforementioned designs are using  $l$  duplications of SC decoder for LSC decoder with list size  $l$ . Consequently, compared with SC decoder, the complexity of LSC increases from  $n \log n$  to  $l \cdot n \log n$ , where  $n$  and  $l$  are the length of codeword and list size, respectively. However, such complexity increasing makes all current existing LSC architectures are impractical for decoders with large list size.

This paper presents a hardware design approach for LSC decoding using path-overlapping to maximize hardware efficiency for optimal energy utility. Instead of using  $l$  copies of SC decoder for LSC decoder, only one SC decoder used in our design. The calculations associated with each path occur simultaneously in the same decoder by carefully arranging the hardware configuration and scheduling of SC decoding. We arrange the LLR calculations of each path instantiated to occupy the decoder hardware stages serially in a streamlined

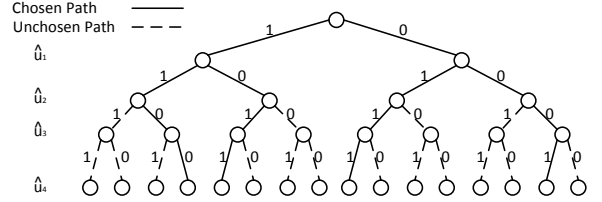


Fig. 1. An example of LSC decoding with list size 4 for (8, 4) polar code from codeword tree aspect

fashion. This yields a significant reduction of hardware complexity. We also analyze and mitigate the latency overhead incurred in the path-overlapping scheme. Three approaches developed to reduce this overhead are: multi-decision LSC decoding, path-LLR-compute-ahead scheme and adaptive LSC decoding. The simulation results show that with proposed approach, the widely proposed LSC decoder can achieve a significantly higher hardware efficiency. For instance, for LSC decoder with code length  $n = 1024$  and list size  $l = 4$ , at least 50% hardware efficiency improvement achieved with proposed design approach, and the maximum improvement is up to around 130%.

This paper is organized as follows. The relative background is reviewed in section II. In following, the proposed approach is described in section III. After that, the hardware efficiency performance and relevant analysis are presented in section IV. Finally, this paper is concluded in section V.

## II. BACKGROUND

### A. Polar Code

As introduced in [1], a polar code is constructed by successively performing channel polarization. Mathematically, polar codes are linear block codes of length  $N = 2^n$ . The transmitted codeword  $\mathbf{x} \triangleq (x_1, x_2, \dots, x_N)$  is computed by  $\mathbf{x} = \mathbf{u}\mathbf{G}$  where  $\mathbf{G} = \mathbf{F}^{\otimes m}$ , and  $\mathbf{F}^{\otimes m}$  is the  $m$ -th Kronecker power of  $\mathbf{F} = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix}$ . Each row of  $\mathbf{G}$  is corresponding to an equivalent polarizing channel. For an  $(N, k)$  polar code,  $k$  bits that carry source information in  $\mathbf{u}$  are called information bits. They are transmitted via the most  $k$  reliable channels. While the rest  $N - k$  bits, called frozen bits, are set to zeros and are placed at the least  $N - k$  reliable channels.

Polar codes can be decoded by recursively applying successive cancellation to estimate  $\hat{u}_i$  using the channel output  $y_0^{N-1}$  and the previously estimated bits  $\hat{u}_0^{i-1}$ . The calculation starts from channel output to the codeword, and is computed stage by stage. Polar code with length  $n$  has  $\log_2 n$  stages. The previously estimated bits for intermediate stages are called partial sum. This decoding process of polar code can be regarded as the path searching in the code tree. SC decoding

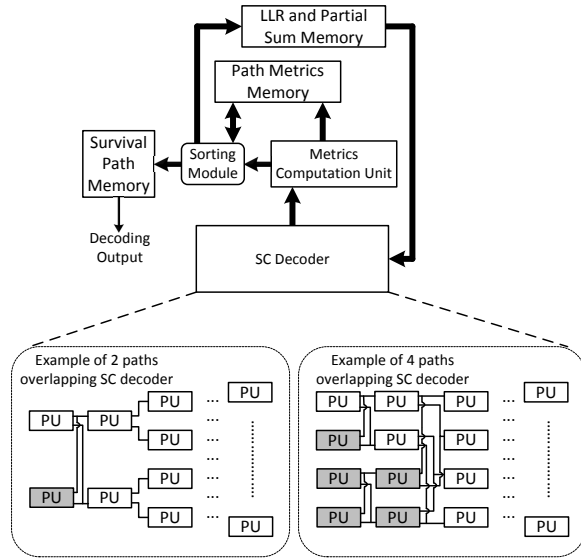


Fig. 2. The architecture of proposed design

reserves only one survival path every layer. If multiple paths are reserved in every layer, it is LSC decoding. The more paths survive, the higher chances the correct codeword can be found. Fig. 1 shows an example of LSC decoding with list size 4 for (8, 4) polar code from codeword tree aspect.

### B. Conventional architecture of LSC

For the LSC algorithm, every information bit can derive two candidate paths, which are used to represent the decision of bit as 0 or 1. Each path has its own path metric which is corresponding to its survival probability. When performing the LSC decoding,  $l$  paths are expanded to  $2l$  paths for each estimated information bits. Then the metrics of  $2l$  paths are calculated to decide the  $l$  survivals. All the corresponding inner log likelihood ratios (LLRs) and partial sum of the reserved paths need to be kept along with  $l$  paths as well. Finally, the  $l$  paths are fed back to SC decoders and do all the steps again and again until the last information bit is decoded.

Although all the LSC designs mentioned in Section I have differences at some details, the main architecture are similar. Typically, for a LSC decoder, it has  $l$  copies of SC decoders and one metrics computation units (MCU), one sorting module and three memory banks with respect to path metrics, current survival paths and LLRs and partial sums. The SC decoder consists of multiple processing units (PUs) with a tree architecture which consumes most of hardware resources. Such duplications of SC decoder yield a significant hardware redundancy of LSC decoder design. In our proposed design, we are trying to avoid such unnecessary redundancy.

## III. PROPOSED APPROACH

In this section we present our path-overlapping approach and discuss how performance optimization is carried out. Fig. 2 shows the architecture of proposed approach and the examples of the modified architecture of SC decoders associated with the list sizes two and four. Since the duplications of SC decoder involves the most hardware complexity, we removed all the copies and kept only one SC decoder. However, this modification of architecture does not mean that we just simply change parallel computing to a single-threaded lazy serial

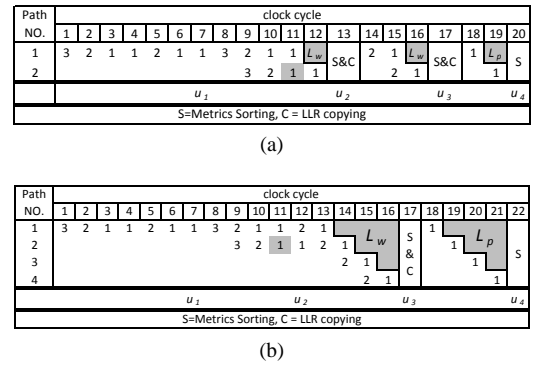


Fig. 3. Decoding schedule of the path-overlapping scheme for (8, 4) polar code with (a) list size = 2 and (b) list size = 4

approach that computes one path at a time. Instead, every path is computed simultaneously in the decoding threads by judiciously utilizing the decoder hardware as follows: The processing timing of each path is overlapped with others in the pipeline arrangement. The architecture of SC decoder is modified to support this new paradigm. Since modifications are made only on architecture and scheduling plan, no decoding performance gain loss or change is incurred. The sorting module, MCU, and related memory components are compatible with other LSC decoders, and the partial sum generator is scheduled a similar way to be compatible with the path-overlapping SC decoder. Thus we do not discuss that in this paper. In the next subsections, the details of the scheme and the specific SC decoder are discussed.

### A. Path-Overlapping Scheme and Relevant Analysis

Simultaneous processing approach is already presented in some SC decoders, and it is used for multiple frames in order to increase the throughput [8]. The SC decoder with tree architecture consists of multiple processing units (PU) arranged like a binary tree. For every clock cycle, only one stage of PUs in the tree is activated. The basic idea of simultaneous processing approach is activating multiple decoding stages in one clock cycle by feeding in several frames in pipeline. This means that each frame comes into the decoder with one clock cycle delay.

Stemming from above idea, we realize that the duplications of SC decoder in conventional LSC decoder is unnecessary. All the paths can be fed into the same decoder in pipelined fashion. Different stages in the single SC decoder can process different paths simultaneously. Computations of successive paths are overlapped in temporal with only one clock cycle delay. However, the decoding scheme is not exactly the same as multiple frames overlapping SC decoder. Fig. 3a and Fig. 3b show the decoding schedule of two and four path-overlapping scheme, respectively. The number means current activated stages, and the duplicated stage is marked with gray. According to [8], if a SC decoder is with  $l$  path-overlapping scheme, where  $l \leq (2^i - 1)$ , it can be constructed by duplicating  $(2^{i-1} - 1)$  stages, where the index starts from the information bits side with respect to the tree architecture. The duplication plan is also presented in Fig. 2. Noticeably in Fig. 3b there is only one duplication of stage one, which is not the same as what presented in Fig. 2. This is because the number of copies in Fig. 2 are the minimum requirement for all the case. The actual requirement is decided by the code length and rate. Fig. 3b is just a certain case only one stage duplication is needed for four path-overlapping scheme.

Such architecture significantly reduces hardware complexity. Another advantage of proposed approach is that it can reduce the critical path length of decoder. Usually, the critical path lies in the sorting block. For conventional LSC decoder, the sorting block is composed of staged combination logic. Even for very small list size, e. g. list = 4, the critical path is much longer than any other module. With proposed approach, since each path metrics comes with pipeline arrangement, naturally, the sorting block is designed as a pipeline module which has a shorter critical path than that of combination logic for the same list size. This means, by applying proposed approach, LSC decoder can run at a much higher frequency.

Although proposed approach can achieve a higher frequency compared with the conventional LSC decoder, there are some additional clock cycles introduced. These consist of two parts. The first part is the path pipeline latency  $L_p$ . Since all the paths are fed into decoder with one clock cycle delay, for the LSC with list size  $l$ ,  $L_p = (l - 1)$ . The second part is path waiting latency  $L_w$ . After the number of path extending to the maximum, the pipeline processing has to suspend when estimating the newly generated information bit since the decoder needs to wait for all the paths to finish before commencing metric sorting and LLR copying. This waiting period is referred to as pipeline stalling. The waiting time is equal to  $L_p$ . Thus, for the list size  $l$  LSC with respect to  $(n, k)$  polar code,  $L_w = (k - \log_2 l - 1) \cdot (l - 1)$ . Thus, the total latency overhead introduced by path-overlapping scheme  $L_m$  can be calculated by:

$$L_m = L_w + L_p = (k - \log_2 l) \cdot (l - 1). \quad (1)$$

This design approach can be applied to any current existing LSC decoders. It significantly reduce the hardware complexity by eliminating redundant instances, and it incurs few additional clock cycles to achieve the improvement. Thus, it is difficult to evaluate such design approach merely in term of the usage of hardware resource or the latency. Thus we introduce the hardware efficiency (HE) metric which is noted as  $e$  to measure the performance of proposed approach. The  $e$  is defined as:  $e = \text{Throughput}/\text{Area}$ .

From Eq. (1), we can tell that the latency overhead would significantly aggregate with either list size or code rate, which can significantly diminish the  $e$ . In order to achieve a high  $e$  with proposed approach, the latency overhead must be reduced to an acceptable level. In the next sections, we will present three approaches aimed at decreasing the latency overhead.

### B. Latency Reduction via Multi-Decision List SC Decoding

The first part of Eq. (1) corresponds to the path waiting latency. For every instance of estimating an information bit, the pipeline processing has to suspend until all the paths finish calculations. This provides an observation that if the times of estimating the information bit can be reduced, the  $L_w$  will decrease significantly.

Multi-decision is an approach of estimating  $m$  bits ( $m > 1$ ) instead of just one at the same time. It helps to reduce the number of estimations. Many approaches can be regarded as multi-decision [7] [9] [10] [11]. Generally, they can be classified into two types. The first type is referred to as regular mutil-decision decoder; it estimates  $m$  bits ( $m > 0$ ) every time. Most of current multi-decision decoders belong to this type [7] [9]. The second type is called irregular mutil-decision decoders; the number of bits estimated every time is not fixed. Currently, only the list fast-SSC decoder [11] belong to this type. It simplifies the SC decoding by finding certain pattern in

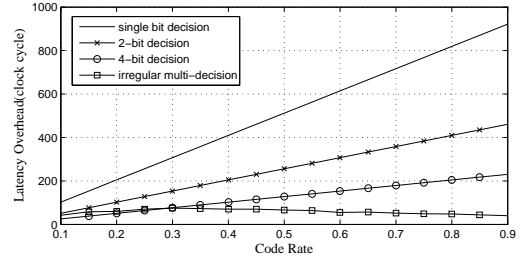


Fig. 4. latency overhead for different scheme

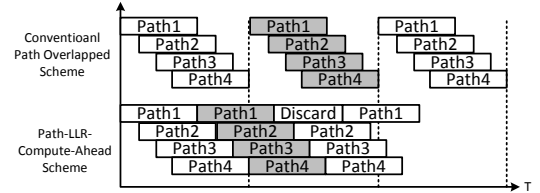


Fig. 5. decoding schedule of path-LLR-compute-ahead scheme

the codewords. Such subcodes with certain pattern also refer to constituent codes. The number of bits estimated every time is corresponding to the size of constituent code. Besides, the distribution of constituent codes irregularly change along with code rate.

For path-overlapping LSC decoder with mutil-decision,  $L_m$  can be further reduced to  $L_m = \alpha \cdot (l - 1)$ . For  $m$  bits regular mutil-decision,  $\alpha = \lceil (k - \log_2 l) / m \rceil$ . For irregular mutil-decision,  $\alpha = S - \log_2 l$  where  $S$  is the total number of constituent codes which irregularly changes along with code rate. Fig. 4 shows the latency overhead of different schemes for LSC decoder with code length  $n = 1024$  and list size  $l = 4$ . We can see that all the mutil-decision schemes can significantly reduce latency overhead, and as increasing of code rate, the irregular mutil-decision scheme can still keep a very low latency overhead.

### C. Latency Reduction via Path-LLR-Compute-Ahead Scheme

Besides reducing the number of estimations, the other approach to decrease latency overhead is by avoiding the pipeline stalling. This can be done via path-LLR-compute-ahead scheme (PLCAS). Fig. 5 shows this decoding schedule. A single bar means the decoding process between estimations of two successive information bits. When pipeline stalling happens in one path, instead of waiting, current path can do a pre-estimated between two candidates (0 and 1) which it solely generates without suspension. The pipeline processing continues with the one with larger metrics and keeps the other to compared with the next coming paths. If more suitable paths are found later, the previous computed ones are discarded. With this scheme, the  $L_m$  for the best case is equal to pipeline latency  $L_p$ , which means the entire processing is handled without any stalling, and the  $L_m$  for the worst case is equal to simple path-overlapping scheme.

### D. Latency Reduction via Adaptive LSC Decoding

In Eq. (1), the second part of the formulation is equal to the  $L_p$ . It is determined by the number of paths set in the pipeline. This makes the latency overhead increases linearly with respect to the list size  $l$ . If we can decrease the value, the latency overhead can be significantly reduced. Typically,  $L_p$  is fixed

for a LSC with given length. However, by applying adaptive LSC algorithm [12], the  $L_p$  is allowed to change on the fly according to current metrics of each path. The list size would decrease along the decoding processing, which also means the latency overhead would get reduction.

In [12], basic hardware architecture is also proposed. Even though the list size would decrease along the decoding processing, the architecture proposed in [12] still needs  $l$  copies of SC decoder for its initial status. The usage of hardware resource is same as regular LSC decoder. Proposed approach can exploit the metric of adaptive LSC decoder via cutting down the unnecessary hardware complexity. With proposed approach there is no redundant hardware even when the list size decrease. Such property allows adaptive LSC decoder to benefit more in term of  $e$ . This will be shown in section. IV.

#### IV. PERFORMANCE AND ANALYSIS

Fig. 6 shows the improvement of  $e$  with proposed design approach for widely proposed LSC decoders with code length  $n = 1024$  and list size  $l = 4$ . The x-axis is the rate of polar code, and the y-axis is the ratio of  $e$  with proposed approach over  $e$  with ordinary approach. The  $e$  with ordinary approach for a given LSC decoder has a consistent value. We apply proposed approach to four types of LSC decoder. They are conventional LSC decoder which also is regarded as 1-bit decision LSC decoder, 4-bit decision LSC decoder, irregular multi-bit decision decoder and the adaptive LSC decoder. We also calculated the upper and lower bound of the  $e$  improvement with PLCAS. These simulations are based on the decoders described in [4], [7], [11] and [10], the related synthesis results and the analysis we made in the previous sections.

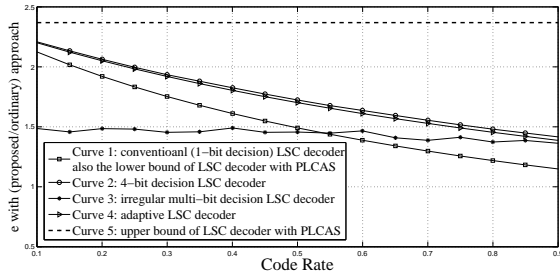


Fig. 6. the improvement of  $e$  with proposed design approach

In Fig. 6, all the curves are beyond the ratio of one, which means with the proposed approach, all the decoders are able to achieve a better hardware efficiency. According to curve 1 and curve 2, the hardware efficiency of regular decision decoder, 1-bit and 4-bit decision decoder, is decreasing along with the code rate increasing. This is because the latency overhead is larger at higher code rate. Besides, the regular multi-bit (4-bit) decoder achieves more improvement of  $e$  than that of conventional (1-bit) decoder, which is due to the latency reduction as we described in section III-B. This can easily derive that for  $n$ -bit-decision regular decoder, the bigger the  $n$ , the more the improvement of  $e$  can be achieved with proposed approach. Curve 1 and 5 indicate the range of the  $e$  improvement with PLCAS. The actual value depends on the channel outputs and channel quality. According to curve 4 and curve 1, we can tell that the adaptive LSC help proposed approach to dramatically increase the hardware efficiency. Such increasing benefits from the decreasing of latency overhead as we analyze in section III-D. Another very

interesting phenomenon is about the improvement of irregular multi-bit decision (list fast-SSC decoder). The gain of  $e$  does not change too much with code rate varying. This is because the latency overhead of irregular multi-bit decision decoder does not linearly change along with coder rate. The average improvement of irregular multi-bit decision is less than that of regular one. This is due to the inherent latency of irregular LSC decoder is already very low [10].

Noticeably all the improvements are calculated based on the assumption that the maximum frequency of decoder with proposed approach or ordinary approach are the same. However, according to the analysis in section III-A, the maximum frequency of decoder with proposed approach should be higher, which indicates that the improvements of  $e$  in Fig. 6 should be even more in practice. Additionally, all the approaches mentioned above are not conflicting with each other. Using multiple approaches together can further increase the hardware efficiency. The above mentioned properties indicate that proposed approach can measurably contain the hardware complexity associated with large scale LSC decoder implementation.

#### V. CONCLUSION

This paper presents a novel design approach to improve the hardware efficiency of LSC decoder via path-overlapping scheme. The details of design approach and three strategies to reduce the latency overhead are also presented. The numerical results show that the conventionally used LSC decoders can significantly achieve a higher hardware efficiency using the proposed approach.

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